REMARKS

Claims 1 and 4 are amended. No new subject matter is added. Reconsideration and allowance of claims 1-12 is requested in light of the following remarks.

Allowable Subject Matter

Claims 3, 7 and 9-12 are objected to as being dependent upon a rejected base claim, but are otherwise indicated to be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

At this time, the applicant wishes to retain claims 3, 7 and 9-12 in their present form so that the comments presented below may be fully considered.

Claim Rejections – 35 U.S.C. § 103

Claims 1, 2, 4-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,899,742 to Sun ("Sun") in view of U.S. Patent Application Publication No. 2002/0109196 to Fujisawa, et al. ("Fujisawa"). The applicant disagrees.

Claim 1 is amended to recite a first silicide layer. This feature is fully supported by the original application at, e.g., claim 1. The change is necessary because claim 4 also recites a silicide layer, and thus a proper antecedent basis is required.

Claim 1 is directed at a semiconductor device, not a method of manufacturing a semiconductor device. Sun is alleged to teach a blocking insulation layer 44 (FIG. 3H) as recited in claim 1. However, contrary to claim 1, Sun's completed semiconductor device (FIG. 3H) does not show that the alleged blocking insulation layer 44 is disposed on a portion of the active region neighboring the alleged isolation layer 31.

It is recognized that Sun fails to disclose the recited alignment structure between the recited first silicide layer, the recited blocking insulation layer, and the recited spacer. Rather, Fujisawa is alleged to disclose the recited alignment structure with silicide layer 7, isolation region 2, blocking insulation layer 8, and spacer 5. However, contrary to claim 1, Fujisawa's FIG. 2 shows that the alleged silicide layer 7 does not have a boundary that is aligned with an edge of the alleged blocking insulation layer 8. The boundary of Fujisawa's silicide layer 7 is instead aligned with an edge of with the isolation region 2 (FIG. 2).

For the above reasons, the Sun/Fujisawa combination fails to establish *prima facie* obviousness for claim 1 because it does not teach or suggest all the features recited in the claim. MPEP 2131.

Claims 2 and 4 are allowable over the Sun/Fujisawa combination at least because any claim that depends from a nonobvious independent claim is also nonobvious. MPEP 2143.03.

Claim 4 is amended to recite a second silicide layer. This change is fully supported by the original application at, e.g., claim 4. Contrary to claim 4, neither Sun nor Fujisawa discloses a second silicide layer disposed on a top surface of the gate pattern. For this additional reason, the Sun/Fujisawa combination fails to establish *prima facie* obviousness for claim 4. MPEP 2143.03.

Regarding claim 5, similar to claim 1 it recites that the silicide layer has a boundary aligned to the edge of the blocking insulation layer and a boundary aligned to the edge of the sidewall spacer. It was explained above with regard to claim 1 that both Sun and Fujisawa fail to teach or suggest this feature. Consequently, the Sun/Fujisawa combination fails to establish *prima facie* obviousness for claim 5 because it does not teach or suggest all the features recited in the claim. MPEP 2143.03.

Claims 6 and 8 are allowable over the Sun/Fujisawa combination at least because any claim that depends from a nonobvious independent claim is also allowable. MPEP 2143.03.

Furthermore, claim 6 recites that forming the spacer insulation layer includes stacking a silicon nitride layer and a silicon oxide layer. Contrary to this feature, neither Sun (FIG. 3G) nor Fujisawa (FIG. 2) indicate that the alleged sidewall spacers (Sun's 37e, 37a, 37c, 37d; Fujisawa's 5) are formed of a stacked silicon nitride layer and a stacked silicon oxide layer.

For this additional reason, the Sun/Fujisawa combination fails to establish *prima facie* obviousness for claim 6 because it does not teach or suggest all the features recited in the claim. MPEP 2143.03.

Furthermore, claim 8 recites that forming the spacer insulation layer includes conformally forming a silicon nitride layer on the semiconductor substrate and forming a silicon oxide layer on the silicon nitride layer. Contrary to this feature, neither Sun (FIG. 3G) nor Fujisawa (FIG. 2) indicate that the alleged sidewall spacers (Sun's 37e, 37a, 37c, 37d; Fujisawa's 5) are formed of a silicon nitride layer that is conformally formed on the substrate and silicon oxide layer that is formed on the silicon nitride layer.

For this additional reason, the Sun/Fujisawa combination fails to establish *prima facie* obviousness for claim 8 because it does not teach or suggest all the features recited in the claim. MPEP 2143.03.

Conclusion

For the above reasons, reconsideration and allowance of claims 1-12 is requested. Please telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Todd J. Iverson
Reg. No. 53,057

MARGER JOHNSON & McCOLLOM, P.C.
210 SW Morrison Street, Suite 400
Portland, OR 97204
503-222-3613
Customer No. 20575

I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (571) 273-8300 on November 10, 2005.

Li Mei Vermilya